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1. An image forming apparatus comprising:

a semiconductor laser;

an optical unit which scans a rotational photo conductor by a laser light output by said semiconductor laser; and

a photodetector which detects the laser light output by said semiconductor laser at a predetermined position,

wherein a latent image is formed by scanning said rotational photo conductor based on the laser light detected by the photodetector,

said image forming apparatus further comprising:

a high-frequency clock generation circuit;

a first frequency divider which generates and outputs an image clock which synchronized with an output of said photodetector by dividing a clock output from the high-frequency clock generation circuit; and

an image clock phase changing circuit which changes a phase of the image clock.

2. The image forming apparatus as claimed in claim 1, wherein said high-frequency clock generation circuit comprises:

a voltage controlled oscillator which controls an oscillation frequency of a clock, which is output according to an input signal;

a second frequency divider which divides the clock oscillated by the voltage controlled oscillator;

a phase comparator which compares a phase of the clock output by the frequency divider with a phase of a frequency of a reference clock so as to output a signal corresponding to a result of the comparison,

wherein the signal output by the phase comparator is input to said voltage controlled oscillator.

3. The image forming apparatus as claimed in claim 1, further comprising:

an image data input circuit which inputs image data based on said image clock;

a modulation pattern generation circuit which generates a modulation pattern based on said image data

and the clock output from said high-frequency clock generation means; and

a semiconductor laser control circuit which controls the output of said semiconductor laser based on the modulation pattern generated by the modulation pattern generation means.

4. The image forming apparatus as claimed in claim 3, wherein said first frequency divider, said image clock phase change circuit, said high-frequency clock generator, said image data input circuit and said modulation pattern generation circuit are constituted by an integrated circuit formed in a single semiconductor chip.

5. The image forming apparatus as claimed in claim 4, further comprising a frequency dividing ratio setting circuit which sets a frequency dividing ratio by said frequency dividing means by loading from outside.

6. The image forming apparatus as claimed in claim 4, further comprising a pulse reversal circuit which reverses or forwards a phase of pulses oscillated by said voltage controlled oscillator.

7. The image forming apparatus as claimed in claim 4, further comprising a frequency dividing operation stop and resumption circuit which stops or resumes an operation of said second frequency divider.

8. The image forming apparatus as claimed in claim 6, further comprising a semiconductor laser turn-off circuit which switches off said semiconductor laser at a timing which delays the phase of said pixel clock.

9. An image forming apparatus comprising:

a semiconductor laser;

an optical unit which scans a rotational photo conductor by a laser light output by said semiconductor laser; and

a photodetector which detects the laser light output by said semiconductor laser at a predetermined position,

wherein a latent image is formed by scanning said rotational photo conductor based on the laser light detected by the photodetector,

said image forming apparatus further comprising:

a high-frequency clock generation circuit;

a frequency divider which generates and outputs an image clock which synchronized with an output of said photodetector by dividing a clock output from the high-frequency clock generation circuit;

an image data input circuit which inputs image data based on said image clock;

a semiconductor laser modulation circuit which modulates an output of said semiconductor laser based on a clock output from said high-frequency clock generation means and the image data which input said image data input means; and

a phase change circuit which changes a timing which said image data input means takes in the image data and a phase of said image clock at the same time.

10. The image forming apparatus as claimed in claim 9, wherein said phase change circuit changes the timing for taking in the image data and the phase of the clock of said image clock based on a first synchronous signal at a time of power supply and a turn-off data timing of synchronous signal detection data.

11. The image forming apparatus as claimed in claim 9, wherein said phase change circuit changes the timing for taking in the image data and the phase of said image clock for every scanning timing.

12. The image forming apparatus as claimed in claim 9, wherein said phase change circuit changes the timing for taking in the image data and the phase of said image clock only at a first line of a page.

13. The image forming apparatus as claimed in claim 9, wherein the phase of said image clock is changed when being output, and the timing which said image data input circuit takes in data and a timing which said modulation pattern generating circuit generates a modulation pattern are not changed.

14. An image forming apparatus comprising:

a semiconductor laser;

scanning means for scanning a rotational photo conductor by a laser light output by said semiconductor laser; and

scanning light detecting means for detecting the laser light output by said semiconductor laser at a

predetermined position,

wherein a latent image is formed by scanning said rotational photo conductor based on the laser light detected by the scanning light detecting means,

said image forming apparatus further comprising:

high-frequency clock generation means;

image clock outputting means for generating and outputting an image clock which synchronized with an output of said scanning light detecting means by dividing a clock output from the high-frequency clock generation means; and

image clock phase change means for changing a phase of the image clock.

15. The image forming apparatus as claimed in claim 14, wherein said high-frequency clock generation means comprises:

voltage controlled oscillator means for controlling an oscillation frequency of a clock, which is output according to an input signal;

frequency dividing means for dividing the

clock oscillated by the voltage controlled oscillator means;

phase comparing means for comparing a phase of the clock output by the frequency dividing means with a phase of a frequency of a reference clock so as to output a signal corresponding to a result of the comparison,

wherein the signal output by the phase comparing means is input to said voltage controlled oscillator means.

16. The image forming apparatus as claimed in claim 14, further comprising:

image data input means for inputting image data based on said image clock;

modulation pattern generation means for generating a modulation pattern based on said image data and the clock output from said high-frequency clock generation means; and

semiconductor laser control means for controlling the output of said semiconductor laser based on the modulation pattern generated by the modulation pattern generation means.

17. The image forming apparatus as claimed in claim 16, wherein said image clock output means, said image clock phase change means, said high-frequency clock generator means, said image data input means and said modulation pattern generation means are constituted by an integrated circuit formed in a single semiconductor chip.

18. The image forming apparatus as claimed in claim 17, further comprising frequency dividing ratio setting means for setting a frequency dividing ratio by said frequency dividing means by loading from outside.

19. The image forming apparatus as claimed in claim 17, further comprising pulse reversal means for reversing or forwarding a phase of pulses oscillated by said voltage controlled oscillator means.

20. The image forming apparatus as claimed in claim 17, further comprising frequency dividing operation stop and resumption means for stopping or resuming an operation of said frequency divider.

21. The image forming apparatus as claimed in claim 20, further comprising semiconductor laser turn-off means for switching off said semiconductor laser at a timing which delays the phase of said pixel clock.

22. An image forming apparatus comprising:

a semiconductor laser;

scanning means for scanning a rotational photo conductor by a laser light output by said semiconductor laser; and

scanning light detecting means for detecting the laser light output by said semiconductor laser at a predetermined position,

wherein a latent image is formed by scanning

said rotational photo conductor based on the laser light detected by the scanning light detecting means,

said image forming apparatus further comprising:

high-frequency clock generation means;

image clock output means for generating and outputting an image clock which synchronized with a timing detected by said scanning light detecting means by dividing a clock from said high-frequency clock generation means;

image data input means for inputting image data based on said image clock;

semiconductor laser modulation means for modulating an output of said semiconductor laser based on a clock output from said high-frequency clock generation means and the image data which input said image data input means; and

phase change means for changing a timing, which said image data input means takes in the image data, and a phase of said image clock at the same time.

23. The image forming apparatus as claimed in claim 22, wherein said phase change means changes the timing for taking in the image data and the phase of the clock of said image clock based on a first synchronous signal at a time of power supply and a turn-off data timing of synchronous signal detection data.

24. The image forming apparatus as claimed in claim 22, wherein said phase change means changes the timing for taking in the image data and the phase of said image clock for every scanning timing.

25. The image forming apparatus as claimed in claim 22, wherein said phase change means changes the timing for taking in the image data and the phase of said image clock only at a first line of a page.

26. The image forming apparatus as claimed in claim 9, wherein the phase of said image clock is changed when being output, and the timing which said image data input means takes in data and a timing which said modulation pattern generating means generates a modulation pattern are not changed.

27. An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

a clock phase control circuit which controls a phase of said output pixel clock for each of said lines so as to correct a shift in a write start position in a scanning direction due to a shift in a position of each light-emitting point of said plurality of light fluxes.

28. The image forming apparatus as claimed in claim 27, wherein said clock phase control circuit comprises:

a high-frequency clock generator;

a first frequency divider which generates said output pixel clock by dividing an output of said high-frequency clock generator, the first frequency divider having a circuit which can change a phase of said output pixel clock;

a phase change circuit which changes a phase of said first frequency divider; and

a second frequency divider which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit which can change a phase of said internal clock.

29. The image forming apparatus as claimed in claim 28, wherein said high-frequency clock generator is constituted by a PLL circuit comprising: a voltage controlled oscillator circuit; a programmable counter which divides an output of said voltage controlled

oscillator circuit; and a phase comparator circuit which compares phases of an output of said programmable counter and a reference frequency, wherein said first frequency divider generates said output pixel clock by dividing an output of said voltage controlled oscillator circuit and a phase of said output pixel clock is synchronized with a phase synchronous signal.

30. The image forming apparatus as claimed in claim 29, further comprising a modulation pattern generating circuit which generates a modulation pattern by which an optimum exposure energy is obtained based on the image data in synchronization with said output pixel clock.

31. The image forming apparatus as claimed in claim 30, wherein said modulation pattern generating circuit can change a phase of the output pixel clock for each of a plurality of lines.

32. The image forming apparatus as claimed in claim 31, wherein said first frequency divider, said phase change circuit, said PLL circuit and said modulation pattern generating circuit are formed in a single integrated circuit.

33. The image forming apparatus as claimed in claim 32, wherein said integrated circuit further comprises a semiconductor laser modulation drive circuit.

34. An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

clock phase control means for controlling a phase of said output pixel clock for each of said lines so as to correct a shift in a write start position in a

scanning direction due to a shift in a position of each light-emitting point of said plurality of light fluxes.

35. The image forming apparatus as claimed in claim 34, wherein said clock phase control means comprises:

high-frequency clock generator means;

a first frequency dividing means for generating said output pixel clock by dividing an output of said high-frequency clock generator means, the first frequency dividing means having means for changing a phase of said output pixel clock;

phase change means for changing a phase of said first frequency dividing means; and

second frequency dividing means for generating an internal clock by dividing an output of said high-frequency clock generator, the second frequency dividing means having means for changing a phase of said internal clock.

36. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one of a plurality of lines; and

a clock phase control circuit which controls a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

37. (Amended) The image forming apparatus as claimed in claim 36, wherein said clock phase control circuit comprises:

a high-frequency clock generator;

a first frequency divider which generates said output pixel clock by dividing an output of said high-frequency clock generator, the first frequency divider having a circuit which can change a phase of said output pixel clock;

a phase change circuit which changes a phase of said first frequency divider; and

a second frequency divider which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit which can change a phase of said internal clock.

38. (Amended) The image forming apparatus as claimed in claim 26, wherein said high-frequency clock generator is constituted by a PLL circuit comprising: a voltage controlled oscillator circuit; a programmable counter which divides an output of said voltage controlled oscillator circuit; and a phase comparator circuit which compares phases of an output of said programmable counter and a reference frequency, wherein said first frequency divider generates said output pixel clock by dividing an output of said voltage controlled oscillator circuit and a phase of said output pixel clock is synchronized with a phase synchronous signal.

39. (Amended) The image forming apparatus as claimed in claim 38, further comprising a modulation pattern generating circuit which generates a modulation pattern by

which an optimum exposure energy is obtained based on the image data in synchronization with said output pixel clock.

40. (Amended) The image forming apparatus as claimed in claim 39, wherein said modulation pattern generating circuit can change a phase of the output pixel clock for each of a plurality of lines.

41. (Amended) The image forming apparatus as claimed in claim 40, wherein said first frequency divider, said phase change circuit, said PLL circuit and said modulation pattern generating circuit are formed in a single integrated circuit.

42. (Amended) The image forming apparatus as claimed in claim 41, wherein said integrated circuit further comprises a semiconductor laser modulation drive circuit.

43. (Amended) An image forming apparatus comprising:

an optical scanning unit which scans a plurality of light fluxes on a medium to be scanned by deflecting the light fluxes by a deflector, the light fluxes being synchronous with an output pixel clock and being modulated in accordance with image data of a respective one

of a plurality of lines; and

clock phase control means for controlling a phase of said output pixel clock for each of a plurality of deflecting surfaces of said deflector so as to correct a fluctuation in a scanning length corresponding to the plurality of deflecting surfaces.

44. (Amended) The image forming apparatus as claimed in claim 43, wherein said clock phase control means comprises:

high-frequency clock generator means;

first frequency dividing means for generating said output pixel clock by dividing an output of said high-frequency clock generator means, the first frequency dividing means having means for changing a phase of said output pixel clock;

phase change means for changing a phase of said first frequency dividing means; and

second frequency dividing means for generating an internal clock by dividing an output of said high-frequency clock generator means, the second frequency dividing means having means for changing a phase of said internal clock.